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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/077,767	02/20/2002	Shinya Soeda	401572	3441

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EXAMINER
PRENTY, MARK V

ART UNIT	PAPER NUMBER
2822	5

DATE MAILED: 11/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/077,767	Applicant(s) SOEDA
	Examiner Prenty	Art Unit 2822

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *three* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on *Feb 20, 2002* .

2a) ☐ This action is **FINAL.** 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above, claim(s) _____ is/are withdrawn from consideration.

5) ☒ Claim(s) *10-13* is/are allowed.

6) ☒ Claim(s) *1, 4-7, 9, and 14-16* is/are rejected.

7) ☒ Claim(s) *2, 3, 8, 17, and 18* is/are objected to.

8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☒ The drawing(s) filed on *Feb 20, 2002* is/are a) ☒ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☒ The proposed drawing correction filed on *Feb 20, 2002* is: a) ☒ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☒ All b) ☐ Some* c) ☐ None of:

1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

*See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s). *2*
4) ☐ Interview Summary (PTO-413) Paper No(s). _____
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

This Office Action is in response to the papers filed February 20, 2002.

The drawings filed February 20, 2002 have been approved by the draftsperson.

The drawing amendment filed February 20, 2002 is approved by the examiner.

Claim 5 is rejected under 35 U.S.C. §102(b) as being anticipated by Iwasa (United States Patent 5,686,746, submitted in the Information Disclosure Statement filed February 20, 2002).

With respect to independent claim 5, Iwasa discloses a semiconductor device (see the entire patent, particularly the Fig. 13 disclosure) comprising: a semiconductor substrate 112; a signal interconnection layer 117 on said semiconductor substrate; and a shielding layer 101 (or 108) on at least one side of said signal interconnection layer.

Claim 5 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Iwasa.

Claims 5 and 9 are rejected under 35 U.S.C. §102(b) as being anticipated by Wolfrum et al. (United States Patent 3,373,323).

With respect to independent claim 5, Wolfrum et al. disclose a semiconductor device (see the entire patent, particularly the Figs. 1-3 disclosure) comprising: a semiconductor substrate 1; a signal interconnection layer 13 (or 14) on said semiconductor substrate; and a shielding layer 9 on at least one side of said signal interconnection layer.

Claim 5 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Wolfrum et al.

With respect to dependent claim 9, Wolfrum et al's shielding layer 9 has a fixed potential (see column 6, lines 51-54).

Claim 9 is thus rejected under 35 U.S.C. §102(b) as being anticipated by Wolfrum et al.

Claims 5, 7, 14 and 16 are rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to independent claim 5, Prior Art Figs. 6A/14 illustrate a semiconductor device comprising: a semiconductor substrate; a signal interconnection layer 129 (or 108a) on said semiconductor substrate; and a shielding layer 126a on at least one side of said signal interconnection layer.

Claim 5 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to dependent claim 7, Prior Art Figs. 6A/14's semiconductor device comprises at least one DRAM region and one logic region, including a layer 126 common to a bit line layer in said DRAM region and used as said shielding layer in said logic region.

Claim 7 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to independent claim 14, Prior Art Figs. 6A/14 illustrate a method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising: forming a signal interconnection layer 129 (or 108a) in said logic region; and forming a shielding layer 126/126a on at least one side of said signal interconnection layer in said DRAM region and said logic region.

Claim 14 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to dependent claim 16, Prior Art Figs. 6A/14's shielding layer 126/126a is a bit line layer.

Claim 16 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art

Figs. 6A/14.

Claims 5, 6, 14 and 15 are rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to independent claim 5, Prior Art Figs. 6A/14 illustrate a semiconductor device comprising: a semiconductor substrate; a signal interconnection layer 126a on said semiconductor substrate; and a shielding layer 108a on at least one side of said signal interconnection layer.

Claim 5 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to dependent claim 6, Prior Art Figs. 6A/14's semiconductor device comprises at least one DRAM region and one logic region, including a layer 108 common to a gate electrode layer in said DRAM region and used as said shielding layer in said logic region.

Claim 6 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to independent claim 14, Prior Art Figs. 6A/14 illustrate a method of fabricating a semiconductor device having at least one DRAM region and one logic region and having a signal interconnection layer in said logic region, the method comprising: forming a signal interconnection layer 126a in said logic region; and forming a shielding layer 108a on at least one side of said signal interconnection layer in said DRAM region and said logic region.

Claim 14 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

With respect to dependent claim 15, Prior Art Figs. 6A/14's shielding layer 108a is a gate electrode layer.

Claim 15 is thus rejected under 35 U.S.C. §102 as being anticipated by Prior Art Figs. 6A/14.

Claims 1, 4, 5 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figs. 6A/13 together with Sakai et al. (United States Patent 4,377,819).

With respect to independent claim 1, Prior Art Figs. 6A/13 illustrate a semiconductor device comprising: a semiconductor substrate 100 having a plurality of regions; a resistor group 104/105 including a plurality of resistors located in one of said regions of said semiconductor substrate; and a metal interconnection layer 129 opposite the region in which said resistor group is located.

The difference between Prior Art Figs. 6A/13's semiconductor device and claim 1's semiconductor device is claim 1's semiconductor device further comprises a shielding layer between the resistor group and the metal interconnection layer.

Sakai et al. teach forming a shield over resistors in order to stabilize them (see the entire patent, particularly the Figs. 9-10 disclosure).

It would have been obvious to one skilled in this art to form a shielding layer between Prior Art Figs. 6A/14's resistor group and metal interconnection layer in order to stabilize the resistor group's resistors, as taught by Sakai et al.

Claim 1 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figs. 6A/13 together with Sakai et al.

With respect to dependent claim 4, Sakai et al's shielding layer has a fixed potential (see the entire patent, particularly the Figs. 9-10 disclosure).

Claim 4 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figs. 6A/13 together with Sakai et al.

With respect to independent claim 5, Prior Art Figs. 6A/13 illustrate a semiconductor device comprising: a semiconductor substrate 100; a signal

interconnection layer 129 on said semiconductor substrate; and a resistor group 104/105 including a plurality of resistors.

The difference between Prior Art Figs. 6A/13's semiconductor device and claim 5's semiconductor device is claim 5's semiconductor device further comprises a shielding layer on at least one side of the signal interconnection layer.

Sakai et al. teach forming a shield over resistors in order to stabilize them (see the entire patent, particularly the Figs. 9-10 disclosure).

It would have been obvious to one skilled in this art to form a shielding layer between Prior Art Figs. 6A/13's resistor group and metal interconnection layer in order to stabilize the resistor group's resistors, as taught by Sakai et al.

Claim 5 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figs. 6A/13 together with Sakai et al.

With respect to dependent claim 9, Sakai et al's shielding layer has a fixed potential (see the entire patent, particularly the Figs. 9-10 disclosure).

Claim 9 is thus rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art Figs. 6A/13 together with Sakai et al.

Claim 2 is objected to as being dependent on a rejected base claim (i.e., claim 2 would be allowable over the prior art of record if claim 2 were amended to further include all the limitations of independent claim 1).

Claim 3 is objected to as being dependent on a rejected base claim (i.e., claim 3 would be allowable over the prior art of record if claim 3 were amended to further include all the limitations of independent claim 1).

Claim 8 is objected to as being dependent on a rejected base claim (i.e., claim 8 would be allowable over the prior art of record if claim 8 were amended to further include all the limitations of independent claim 5).

Claim 17 is objected to as being dependent on a rejected base claim (i.e., claim 17 would be allowable over the prior art of record if claim 17 were amended to further include all the limitations of independent claim 14).

Claim 18 is objected to as being dependent on a rejected base claim (i.e., claim 18 would be allowable over the prior art of record if claim 18 were amended to further include all the limitations of independent claim 14).

Claims 10-13 are allowable over the prior art of record.

Registered practitioners can telephone examiner Prenty at (703) 308-4939. Any voicemail message left for the examiner must include the name and registration number of the registered practitioner calling, and the application's Serial Number. Technology Center 2800's general telephone number is (703) 308-0956.

Mark Prenty

Mark V. Prenty

Primary Examiner